What is claimed is:

1. A digital filter circuit comprising:

a first RAM that latches sequentially input data each having a first sampling period;

a second RAM that latches sequentially input data each having a second sampling period;

a first register that latches the data sequentially outputted from the first RAM;

a second register that latches the data sequentially outputted from the second RAM;

a cumulative arithmetic unit that computes the data outputted from the first RAM and the second RAM; and

a selector that alternately outputs the data outputted from the first register and the second register to the cumulative arithmetic unit.

2. A digital filter circuit according to claim 1, which has the function of causing the data having the first sampling frequency or the data having the second sampling frequency to partly disappear by overwriting new data on the data within the first register or the second register.

3. A digital filter circuit according to claim 1, which has the function of feeding back the data computed by the cumulative arithmetic unit to the first register or the second register.

4. A digital filter circuit according to claim 1, wherein the selector is operated to mix the data outputted from the first register or the second register with data outputted from the other register.

5. A digital filter circuit according to claim 1, which has the function of directly inputting the data having the first sampling period to the first register without being latched in the first RAM.

6. A digital filter circuit according to claim 1, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.

7. A data processing method comprising the steps of:

sequentially inputting and latching data each having a first sampling period to and in a first RAM;

sequentially inputting and latching data each having a second sampling period to and in a second RAM;

sequentially outputting and latching the data sent from the first RAM to and in a first register;

sequentially outputting and latching the data sent from the second RAM to and in a second register;

alternately outputting the data from the first register and the second register to a cumulative arithmetic unit; and

computing the data outputted to the cumulative arithmetic

unit.

8. A data processing method according to claim 7, further comprising the step of causing the data having the first sampling frequency or the data having the second sampling frequency to partly disappear by overwriting new data on the data within the first register or the second register.

9. A data processing method according to claim 7, further comprising the step of feeding back the data computed by the cumulative arithmetic unit to the first register or the second register.

10. A data processing method according to claim 7, further comprising the step of mixing the data outputted from the first register or the second register with data outputted from the other register.

11. A data processing method according to claim 7, further comprising the step of directly inputting the data having the first sampling period to the first register without being latched in the first RAM.

12. A data processing method according to claim 7, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.